CLAIMS

What is claimed is:

1) A method of manufacturing a semiconductor device comprising:

a) depositing a first oxide layer over a periphery transistor comprising a gate stack, a drain side sidewall and a source side sidewall and over a core transistor comprising a gate stack, a source side sidewall and a drain side sidewall;

b) etching said first oxide layer wherein a portion of said first oxide layer remains on said source side sidewall and on said drain side sidewall of said periphery transistor and on said source side sidewall and on said drain side sidewall of said core transistor;

c) etching said first oxide layer from said source side sidewall of said core transistor;

d) depositing a second oxide layer over said periphery transistor and said core transistor; and

e) etching said second oxide layer wherein a portion of said second oxide layer remains on said first oxide layer formed on said source side sidewall and on said drain side sidewall of said periphery transistor and wherein said second oxide layer remains on said source side sidewall and on said drain side sidewall of said core transistor.

2) The method as described in Claim 1 wherein said first oxide layer is silicon nitride.

3) The method as described in Claim 1 wherein said first oxide layer is silicon oxide and silicon nitride.

4) The method as described in Claim 1 wherein said second oxide layer is silicon nitride.

5) The method as described in Claim 1 wherein said b) is a chemical etch, wherein said chemical etch does not remove material from said gate stack of said periphery transistor and does not remove material from said gate stack of said core transistor.

6) The method as described in Claim 1 wherein said c) is a self aligned source etch.

7) The method as described in Claim 1 wherein said first oxide layer is thicker than said second oxide layer.

8) The method as described in Claim 1 wherein said core transistor is a flash memory cell.

9) A method for simultaneously manufacturing a wide sidewall spacer on a periphery transistor and a narrow sidewall spacer on a core transistor comprising:

a) depositing a first oxide layer over a periphery transistor comprising a gate stack, a drain side sidewall and a source side sidewall and over a core transistor comprising a gate stack, a source side sidewall and a drain side sidewall;

b) etching said first oxide layer wherein a portion of said first oxide layer remains on said source side sidewall and on said drain side sidewall of said periphery transistor and on said source side sidewall and said drain side sidewall of said core transistor;

c) masking and etching said oxide layer from said source side sidewall and said drain sidewall of said core transistor;

d) depositing a second oxide layer over said periphery transistor and said core transistor; and

e) etching said second oxide layer wherein a portion of said second oxide layer remains on said first oxide layer formed on said source side sidewall and said drain side sidewall of said periphery transistor resulting in a wide sidewall spacer and wherein said second oxide layer remains on said source side sidewall and said drain side sidewall of said core transistor resulting in a narrow sidewall spacer.

10) The method as described in Claim 9 wherein said first oxide layer is silicon nitride.

11) The method as described in Claim 9 wherein said first oxide layer is silicon oxide and silicon nitride.

12) The method as described in Claim 9 wherein said second oxide layer is silicon nitride.

13) The method as described in Claim 9 wherein said b) is a chemical etch, wherein said chemical etch does not remove material from said gate stack of said periphery transistor and does not remove material from said gate stack of said core transistor.

14) The method as described in Claim 9 wherein said first oxide layer is thicker than said second oxide layer.

15) The method as described in Claim 9 wherein said core transistor is a flash memory cell.

16) A method for simultaneously manufacturing a semiconductor comprising a wide sidewall spacer and a narrow sidewall spacer comprising:

a) depositing a first oxide layer over a first transistor comprising a gate stack, a drain side sidewall and a source side sidewall and over a second transistor comprising a gate stack, a source side sidewall and a drain side sidewall;

b) etching said first oxide layer wherein a portion of said first oxide layer remains on said source side sidewall and on said drain side sidewall of said first transistor and on said source side sidewall and on said drain side sidewall of said second transistor;

c) etching said first oxide layer from said source side sidewall of said second transistor;

d) depositing a second oxide layer over said first transistor and said second transistor; and

e) etching said second oxide layer wherein a portion of said second oxide layer remains on said first oxide layer formed on said source side sidewall and on said drain side sidewall of said first transistor and wherein said second oxide layer remains on said source side sidewall and on said drain side sidewall of said second transistor.

17) The method as described in Claim 16 wherein said first oxide transistor is a periphery transistor.

18) The method as described in Claim 16 wherein said second transistor is a core transistor.

19) The method as described in Claim 18 wherein said core transistor is a flash memory cell.

20) The method as described in Claim 16 wherein said first oxide layer comprises silicon oxide and silicon nitride.

21) The method as described in Claim 16 wherein said second oxide layer comprises nitride.

22) The method as described in Claim 16 wherein said c) is a self aligned source etch.

23) The method as described in Claim 16 wherein said first oxide layer is thicker than said second oxide layer.